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Application Note

Voltage References for the CS5012A / CS5014 / CS5016 / CS5101A/ CS5102A / CS5126 Series of A/D Converters

by
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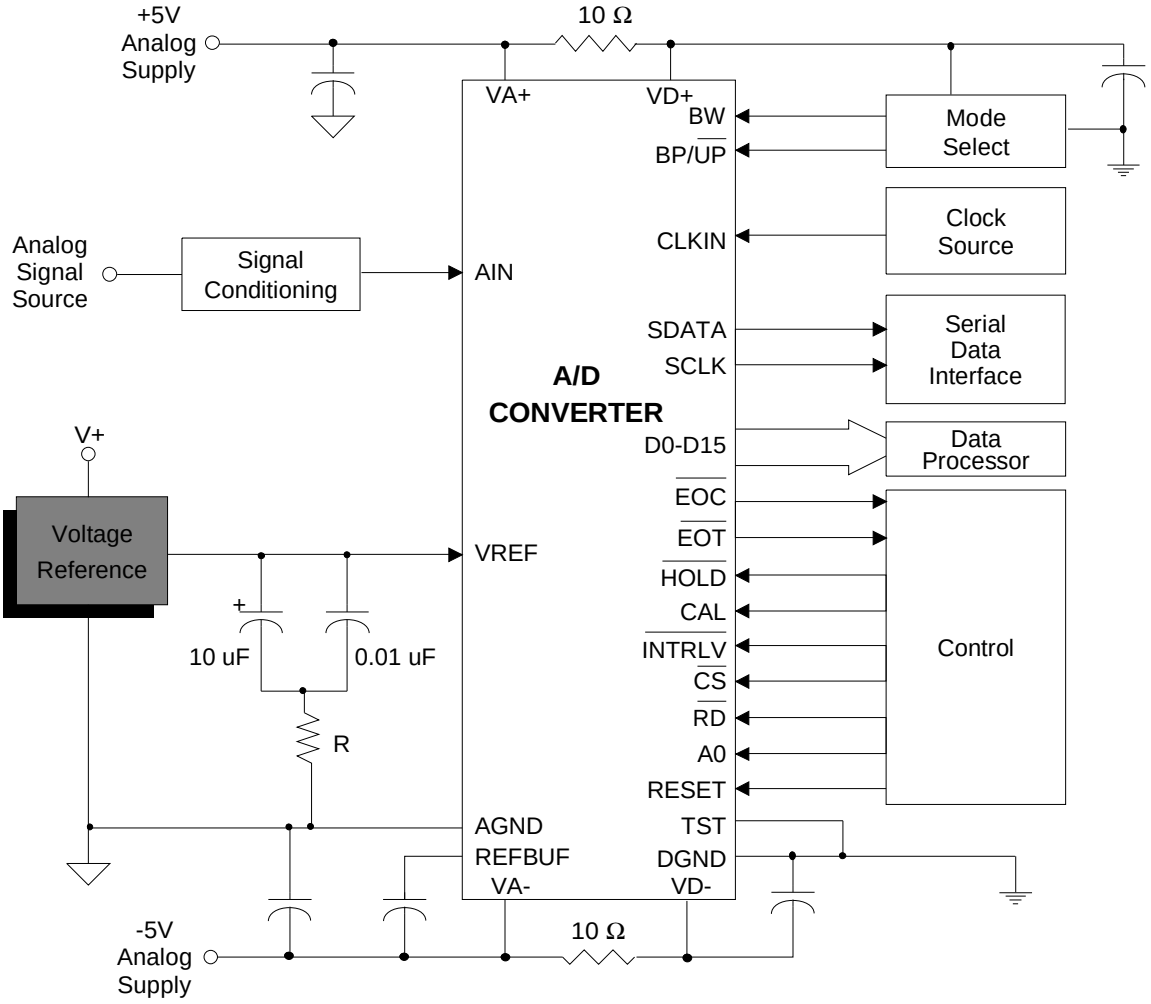

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INTRODUCTION

This application note discusses voltage references for use with Crystal Semiconductor's successive approximation series of A/D converters. Reference design considerations, a design example and suggested reference circuits are explained in detail.

Voltage references provide accurate voltages for use in data acquisition systems in order to establish a basis for conversion. In a data acquisition system, the value of the reference sets the gain of the A/D stage since the digital output corresponds to the ratio of the analog input signal to the reference voltage.

In static applications, information is contained in the signal amplitude, therefore the absolute value of the reference voltage is important. In many signal processing applications, information is contained in the frequency and phase of the signal. Here, absolute value is not as important as the stability of the reference voltage during conversion.

Zener-diode Reference

There are two major varieties of voltage references. The first is the zener-diode based reference which uses a reverse-biased zener diode operated in its breakdown region. Most reference zeners breakdown at voltages between 6.0 and 7.0V, which limits the minimum supply voltage necessary for operation. When the diode is supplied with a constant current, it has a constant voltage drop. Zener references use a zener diode and an integrated feedback amplifier which provides constant current, gain, and buffering for the zener diode.

Zener diodes exhibit two types of breakdown. The first is zener breakdown which has a negative temperature coefficient and is dominant at low current levels. The second, avalanche breakdown, occurs at higher current levels and has a positive temperature coefficient. At some specific current level, these two effects cancel each other and the temperature coefficient of the zener breakdown voltage is zero. As the ambient temperature changes, one of the breakdown mechanisms becomes dominant and the the reverse-biased diode voltage will exhibit a temperature coefficient.

Bandgap Reference

The second major type of reference is the bandgap reference. This reference uses the base-emitter voltage (V_{be}) of a bipolar transistor as a basis for operation. The V_{be} has a negative temperature coefficient (-2mV/°C). This negative temperature coefficient is balanced by a voltage with a positive temperature coefficient of the same magnitude. This voltage is usually obtained by using the difference of two V_{be}'s of transistors operating at different current densities. When both voltages are scaled and summed together, the result is a voltage which is less sensitive to temperature. The headroom required for bias and support circuitry is only a few volts over the output voltage.

Reference Specifications

Voltage references have six important specifications. These are absolute accuracy, temperature coefficient, long-term reference drift, power supply sensitivity, output impedance, and output noise.

Absolute or untrimmed accuracy is the difference between the actual output voltage and the ideal output voltage. It is specified in millivolts.

Temperature coefficient describes the drift in the output voltage with temperature. Since this drift is nonlinear, curve fitting is often used for all temperatures between those actually tested. Voltage references are available with temperature coefficients as low as 1 ppm/°C. Inexpensive references are available with 10 to 50 ppm/°C drift

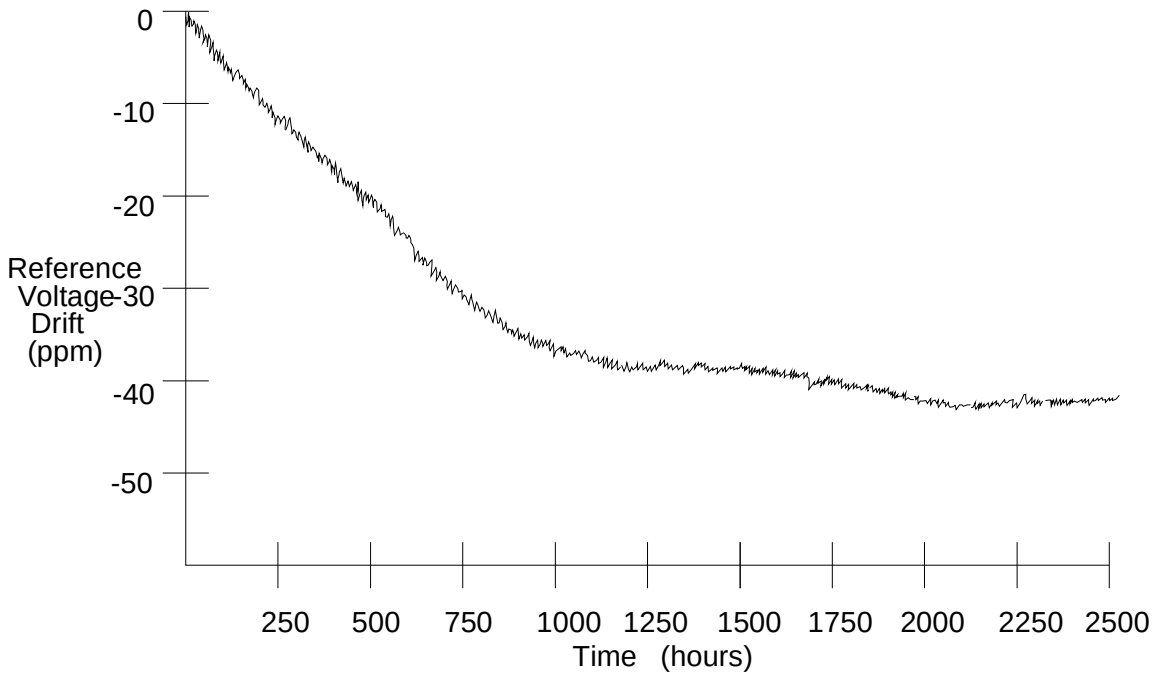


Figure 1. - Long Term Stability of a Typical Zener Reference

which is comparable to on-chip references of bipolar A/D converters. Temperature coefficient is specified in ppm/°C.

Long term stability is the drift in the reference voltage over time. Most references show minor deviations in voltage due to 1/f noise in circuit components. These deviations are usually small and are superimposed on a larger drift characteristic which is due to device aging. An example of this is seen in Figure 1. Long term drift is specified in ppm/1000 hrs.

Power supply sensitivity (line regulation) is the change in output voltage due to a change in power supply. Most references have good power supply rejection at dc, but ac power supply rejection is also important when power supplies are subject to high frequency coupling or noise spikes. PSRR (Power Supply Rejection Ratio) is the ratio of the change in power supply to the change in output voltage. It is specified in dB.

Output impedance is important because of the dynamic loads generated by successive-approximation A/D converters. When the reference is sourcing or sinking current, its output voltage will change due to non-zero output impedance. This impedance must be low enough at all frequencies of interest so the deviation in reference voltage when sourcing current is negligible. Output impedance is specified in ohms.

Output noise can lead to comparison errors in the A/D converter, and subsequently conversion errors. Reference noise is more evident with full scale inputs. It is specified in μV peak-to-peak.

Design Considerations

When interfacing a voltage reference to an A/D converter, the specifications should be robust enough so that the reference does not become a source of conversion error. During conversion, each capacitor of the calibrated capacitor array in the ADC is switched between VREF and AGND in a manner determined by the successive approximation algorithm. The charging and discharging of the array results in a current load at

the reference. The ADC's include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. This buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer. The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the internal buffer. This creates an ac current load as the ADC sequences through conversions.

The reference circuitry must have a low enough output impedance to provide the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Also with CS5012,4,6 converters, bits are converted at a 1MHz rate with a full speed (4MHz) clock. The reference must settle within one microsecond so that it will be accurate before the next bit is converted. Signal amplitude dependent loading and conversion settling time require the output impedance of the reference to remain low from dc to at least 1MHz in order to ensure good converter performance.

The CS5012,4,6 series of converters can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. All CS5012,4,6 converters can actually accept reference voltages up to the positive analog supply. However, the internal buffer's offset may increase as the reference voltage approaches VA+. This increases external drive requirements at VREF. Allowing 250mV headroom for the internal reference buffer is recommended. If the supplies are regulated specifically for the converter, 5.0 volt references may be used if the supply voltages for the ADC are kept between ± 5.25 and ± 5.5 volts.

The magnitude of the current load presented to the external reference circuitry by the ADC's will vary with the master clock frequency. At full speed (4MHz clock), the ADC's require maximum load currents of 10µA peak-to-peak (1µA peak-to-peak typical). The voltage reference must supply this current and maintain adequate voltage regulation. The load currents scale proportionately with the master clock frequency. Slower clocks can be used to relax maximum output impedance specification of the reference.

When driving multiple A/D converters from the same reference circuit, load currents will scale proportionally to the number of converters. Distribute the required decoupling components such that each ADC is locally decoupled.

A reference with a maximum output impedance of 2 Ω will yield a maximum error of 20µV. This reference could drive a CS5016 (LSB=69µV with

Part # \ f_{clk}	4MHz	2MHz	1MHz	500kHz
CS5012 (Vref=4.5V)	27	54	108	216
CS5012 (Vref=2.5V)	15	30	60	120
CS5014 (Vref=4.5V)	7	14	28	56
CS5016 (Vref=4.5V)	2	4	8	16

All units in ohms

Table 1. - Maximum Output Impedance for ≈ 1/4 LSB Reference Deviation

a 4.5V reference) and maintain approximately 1/4 LSB deviation during conversion. Similarly for the CS5014 (LSB=276µV with a 4.5V reference), and CS5012 (LSB=613µV with a 2.5V reference), maximum impedances of 7 and 15 Ω respectively will maintain adequate regulation. Table 1 defines maximum reference impedances allowed for each of the Crystal A/D's operating at different master clock frequencies in order to keep reference deviation approximately equal to 1/4 LSB.

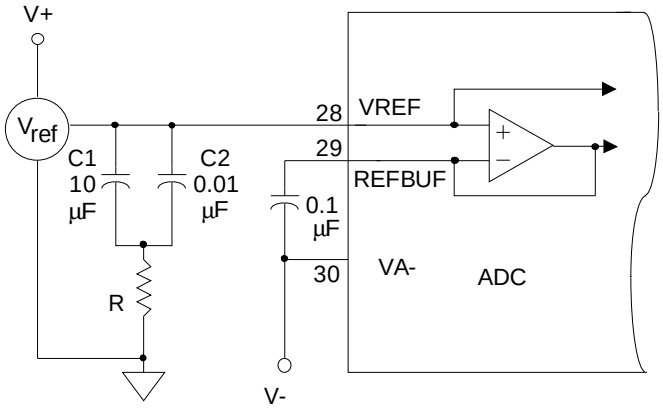
All precision references exhibit extremely low output impedance at dc. However, as frequency increases the impedance also increases. A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum where the reference impedance is too high.

For example, the impedance of an ideal 10µF capacitor drops below 1 Ω at frequencies greater than 16kHz. However, actual capacitors behave differently due to their physical structure. Tantalum-foil electrolytic capacitors begin to appear inductive at frequencies around 100kHz and as a result their impedance begins to rise at frequencies above this. Aluminum electrolytic capacitors appear inductive at frequencies around 10kHz. Ceramic-disk capacitors behave much closer to ideal and begin to appear inductive at frequencies around 5MHz, but 10µF ceramic-disk capacitors are quite rare. Therefore, a high-quality tantalum capacitor (10µF) in parallel with a smaller (0.1µF) ceramic capacitor is recommended. This combination yields low impedance up to frequencies around 50MHz.

Peaking

The presence of large capacitors on the output of some voltage references may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to reduce it.

Most commercially available references use an integrated op-amp to buffer the actual reference generator. External capacitive loading will degrade performance of this op-amp. This degradation can be analyzed using classical analysis techniques. The open loop gain of an ideal op-amp is primarily determined by the internal compensation capacitor which generates a left-half-plane-pole (LHPP) at a very low frequency. The effect of this pole is to reduce the open loop gain by 20dB per decade and to add a -90 degree phase shift to the open loop transfer characteristic. Adding a capacitive load to the output of the op-amp generates another LHPP at a frequency inversely proportional to the capacitor's value. An additional 20dB per decade reduction in gain and -90 degree phase shift result from the second LHPP.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 2. - Reference Connections

The unity gain bandwidth of an op-amp (f_0), is the frequency at which the open loop gain goes to unity. If the total phase shift reaches -180 degrees before f_0 is reached the op-amp will become unstable. The closed loop frequency response peaks at f_0. As the total open loop phase shift at f_0 approaches -180 degrees, the closed loop peak at f_0 approaches infinity. The point of critical damping is the point where the peaking is precisely zero. Any phase shift less than this results in no peaking, and phase shift greater than this results in increased peaking.

Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 2). This resistor adds a left-half-plane-zero (LHPZ) to the open loop characteristic of the op-amp. This zero increases the gain by 20dB per decade, and adds a +90 degree phase shift. The resulting reduction in total phase shift at f_0 reduces peaking in the closed loop characteristic. The equation in Figure 2 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

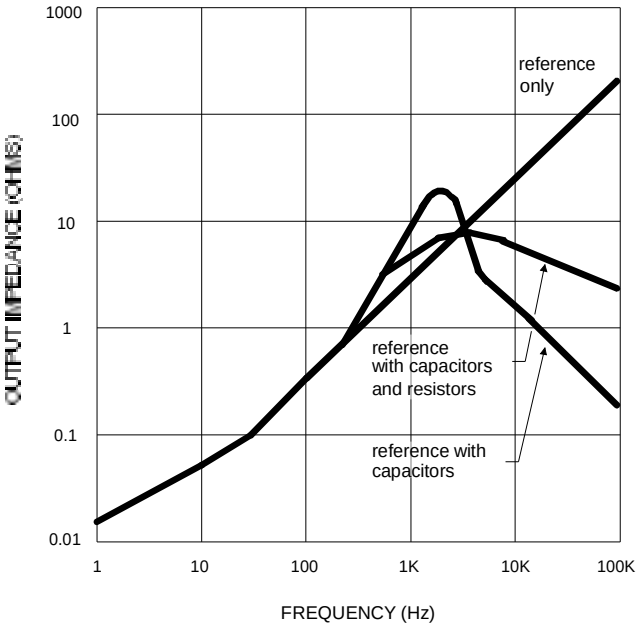


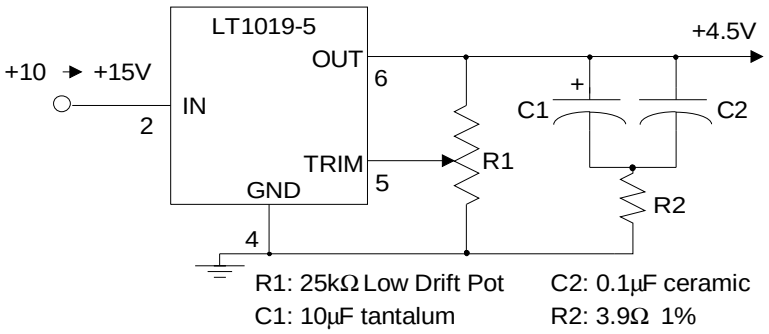
Figure 3. - Output Impedance Curves for LT1019-5

Design Example

Figure 3 shows the output impedance characteristic of an LT1019-5 reference trimmed to 4.5V. The three curves represent impedances of the stand-alone reference, the reference with a 10μF tantalum and a 0.1μF ceramic capacitor added in parallel to the output, and the reference with the capacitors and a 2.2 Ω resistor in series with them (See Figure 2). Without loading, the reference impedance rises above 100 Ω at 50kHz. Adding the capacitors, peaking can be seen, but the maximum impedance is about 13 Ω at 4kHz. As shown in Table 1, 13 Ω is sufficient for use with the 12-bit converters and for the 14 and 16-bit converters with slow master clocks. With the addition of the 2.2 Ω resistor, the peak is reduced to 6 Ω and the impedance approaches 2.2 Ω at high frequencies.

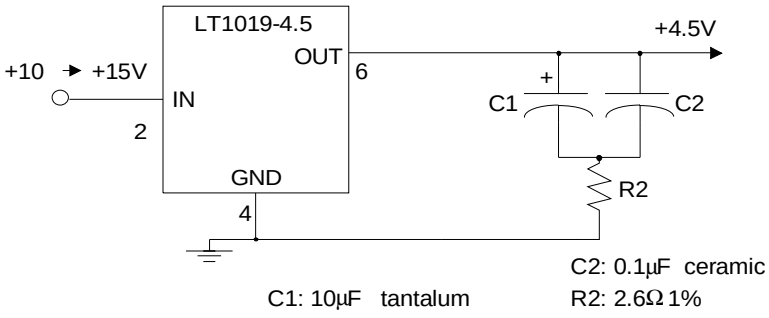
Suggested Voltage Reference Circuits

Nine reference circuits were characterized for use with the CS5012, CS5014, CS5016, CS5101, CS5102, CS5126 family of successive-approximation A/D converters. Important reference specifications such as output impedance and drift were measured for all references using standard test techniques. In addition, a Fast-Fourier Transform (FFT) test was performed to characterize the total dynamic performance of each reference circuit while driving a CS5016 converter. The same CS5016 was used for all tests yielding results which allow the comparison between different references. A summary of performance can be seen in the table at the end of this application note. During the FFT test, a pure sine wave is applied to the CS5016 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the waveform and distributes its energy among 512 "frequency bins". Distribution of energy in bins outside of the fundamental and dc can be attributed to errors in the A/D converter's performance, the reference, or the input sine wave.



Reference Type	Bandgap
Untrimmed Accuracy	2.5mV
Max Impedance	6.5Ω @ 3.2KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	250µV p-p
S / (N+D) (100Hz)	89dB
S / (N+D) (1kHz)	89dB

Figure 4. LT1019-5 Reference Trimmable to 4.5V



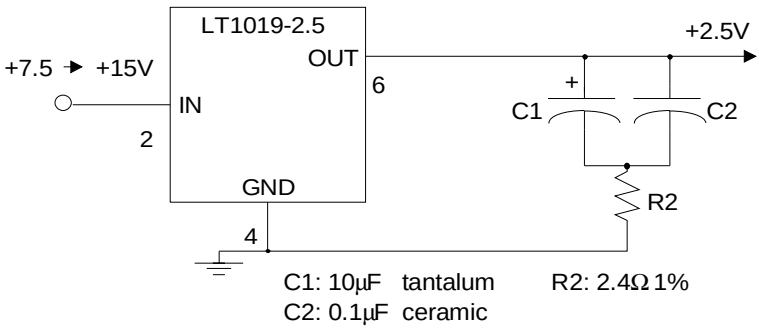
Reference Type	Bandgap
Untrimmed Accuracy	3.0mV
Max Impedance	3.1Ω @ 6.1KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	150µV p-p
S / (N+D) (100Hz)	91dB
S / (N+D) (1kHz)	90dB

Figure 5. LT1019-4.5 Reference

The result of the FFT test is the ratio of input signal amplitude to the combination of harmonic distortion and total integrated noise. It is referred to as S/(N+D) in all of the performance charts in Figures 4 to 10. This ratio is expressed in dB. If input sine wave distortion and the actual A/D converter's distortion and noise are assumed to be negligible, the S/(N+D) is due to the reference only. In reality, this assumption can not be made. In the case of the Great Reference (See Figure 11), performance matches or exceeds the capability of the test setup. S/(N+D) ratios of 72 and 82 dB are sufficient for the 12-bit and 14-bit converters. For the 16-bit converters, 88 to 94 dB is necessary.

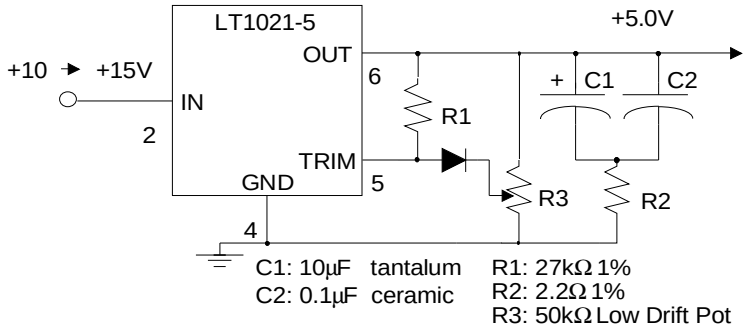
FFT tests were performed at 100Hz and 1kHz. The 100Hz test checks the output impedance of the reference chip itself which dominates at low frequencies. The 1kHz FFT test checks the output impedance at intermediate frequencies in the kHz range. The highest output impedance was seen in all references at these intermediate frequencies. Since the reference capacitors dominate the impedance at high frequencies, high frequency FFT tests were not necessary. Although not tested, the best reference is likely to yield the best DNL performance.

The least complicated reference circuit is the stand-alone reference chip with a passive compensation network. Its temperature drift and noise performance is equal to the reference chip itself since the compensation network does not change the dc output voltage. Keeping the output impedance low from dc to 1MHz is not trivial however, since there is no additional active circuitry added to perform this task. Five references were tested in the stand-alone configuration. Figures 4, 5, 6, 7, and 8 illustrate schematics and measured specifications for these references. All references are monolithic with the exception of the VRE104 reference which is a hybrid (available from Thaler (602) 742-5572). Notice that the VRE104



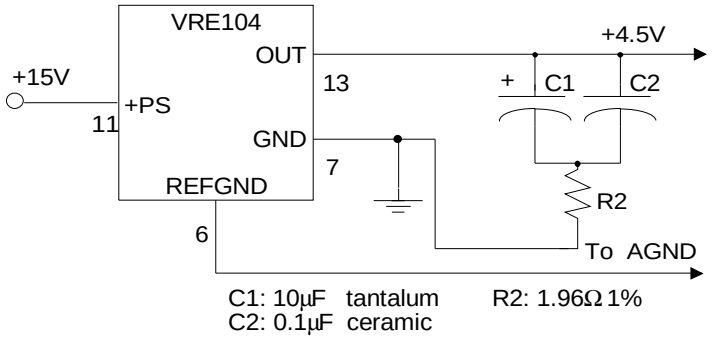
Reference Type	Bandgap
Untrimmed Accuracy	1.25mV
Max Impedance	4.0Ω @ 5.8KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100µV p-p
S / (N+D) (100Hz)	87dB
S / (N+D) (1kHz)	89dB

Figure 6. LT1019-2.5 Reference



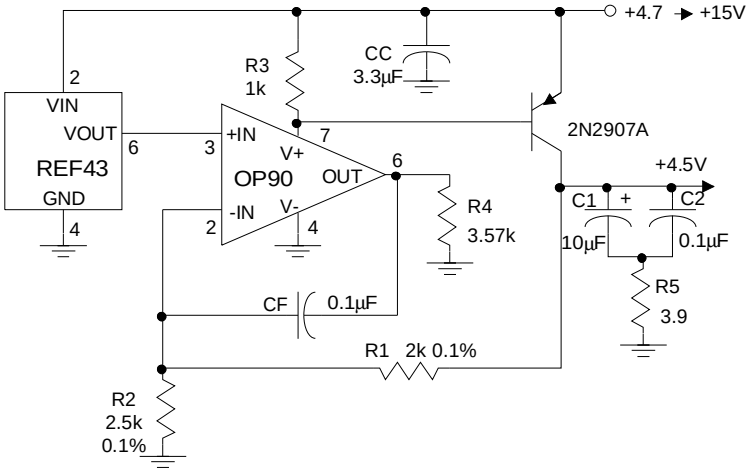
Reference Type	Zener
Untrimmed Accuracy	2.5mV
Max Impedance	3.8Ω @ 5.0KHz
Total Output Drift	3ppm / °C
PSRR (50Hz to 500Hz)	86dB
Long Term Stability	15ppm / 1000hr
Output Noise	60µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 7. LT1021 Reference



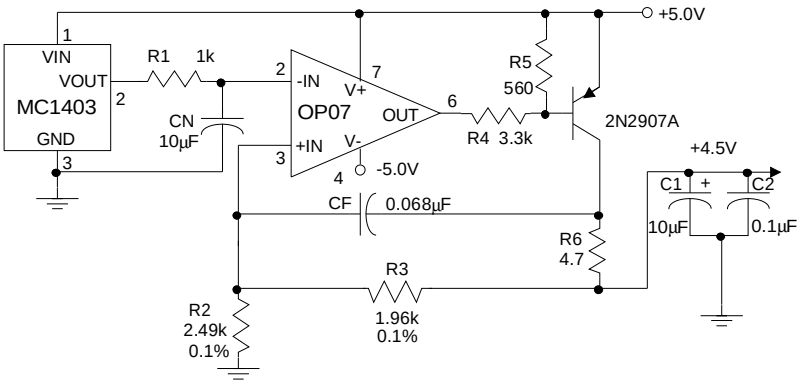
Reference Type	Zener
Untrimmed Accuracy	500µV
Max Impedance	2.5Ω @ 20KHz
Total Output Drift	0.5ppm / °C
PSRR (50Hz to 500Hz)	100dB
Long Term Stability	6ppm / 1000hr
Total Output Noise	80µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 8. VRE104 Reference



Reference Type	Bandgap
Untrimmed Accuracy	1.5mV
Max Impedance	4.4Ω @ 1KHz
Total Output Drift	8.0ppm / °C
PSRR (50Hz to 500Hz)	60dB
Long Term Stability	-
Output Noise (dc to 1MHz)	400µV p-p
S / (N+D) (100Hz)	88dB
S / (N+D) (1kHz)	88dB

Figure 9. Low Power Supply Reference



Reference Type	Bandgap
Untrimmed Accuracy	50mV
Max Impedance	6.9Ω @ 2KHz
Total Output Drift	25ppm / °C
PSRR (50Hz to 500Hz)	80dB
Long Term Stability	-
Output Noise (dc to 1MHz)	30µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 10. Low Headroom Reference

and the LT1019-4.5 require no trimming for 4.5V operation. The calculated value of R2 in each of the references above will change slightly between units. Since the actual variation is small, picking the closest 1% tolerance resistor to the calculated value should give similar performance for all references of a particular manufacturer's model.

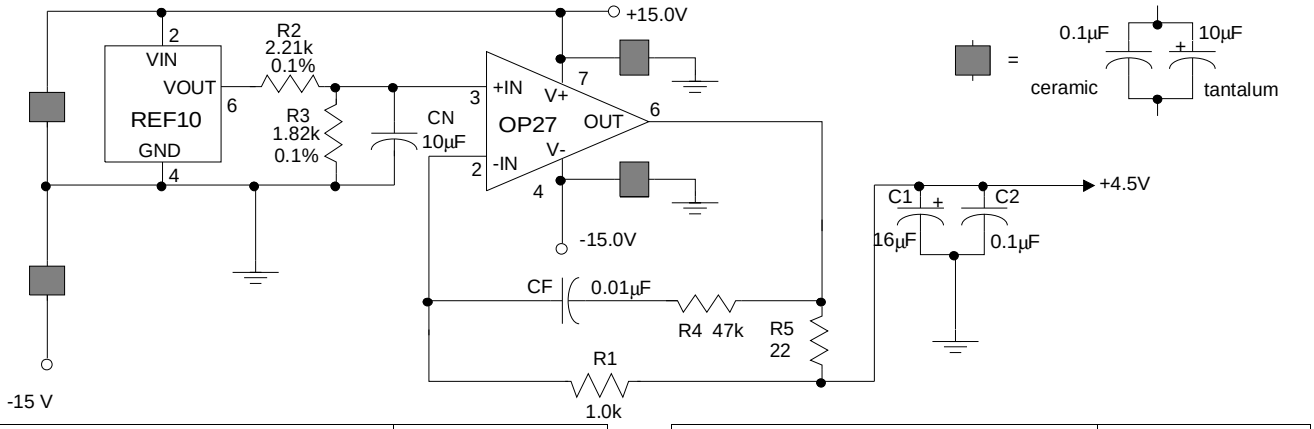
Other stand-alone voltage references with similar specifications include the AD584, REF02, REF03, REF10, and REF43. When designing with these references, the equation shown in Figure 2 should be used to calculate the appropriate value of R2 for each type of reference.

For applications which use ± 5.0 volt supplies, the reference in Figure 9 can be used. This reference circuit, designed by engineers at the former Precision Monolithics, takes advantage of a low power op-amp in a novel feedback configuration to achieve a 4.5 volt reference which operates from 4.7 to 15 volt supplies.

Since only a few microamps of quiescent current flows in the op-amp, it can be assumed that the only current flowing in R3 is the same as that flowing in R4. It can be shown that V6 = 3.57(Vin-V7). For an output of 4.5 volts, and a supply of 4.7 volts, the op-amp has a supply of approximately 4.0 volts and an output voltage of 2.14 volts. This output voltage is well within the maximum specification of the OP-90 op-amp. Other references can be substituted for the REF43 if different drift or noise specifications are required.

The reference shown in Figure 10 is a low noise reference with less than 30µV peak-to-peak of noise from dc to 1MHz. It uses a discrete output stage allowing Vref to come within 300mV of the positive supply. The filtering network R1,CN reduces the bandwidth of the reference and therefore reduces the total output noise. The OP-07 is a low noise op-amp which buffers the filtered reference. This op-amp contributes very little noise to the entire reference circuitry.

The temperature coefficient of this reference is primarily due to to the matching of the gain resistors R2 and R3, so low temperature drift resistors should be used. Long term drift is dominated by the MC1403's drift. Other 2.5 volt references can be used to improve this specification. The output voltage can be changed by adjusting R2 and R3 according to the following equation: Vref = Vout*((R2+R3)/R2). Resistors with 0.1% tolerance for R2 and R3 limit the reference's untrimmed accuracy only. Resistors with 1% or 5% tolerance can be used if untrimmed accuracy less than 50mV is not necessary. The supplies of the



Reference Type	Bandgap
Untrimmed Accuracy	25mV
Max Impedance	0.5Ω @ 3kHz
Total Output Drift	9ppm / °C
PSRR (50Hz to 100Hz)	95dB

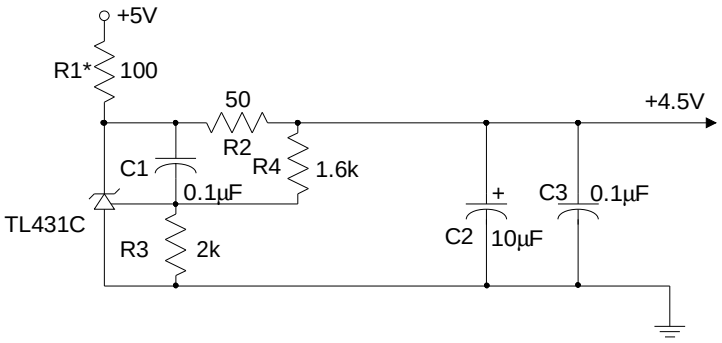
Long Term Stability	50ppm / 1000hr
Output Noise (dc to 1MHz)	5µV p-p
S / (N+D) (100Hz)	92dB
S / (N+D) (1kHz)	92dB

Figure 11. - Great Reference

OP-07 should be bypassed with 0.1µF capacitors to ground.

The reference in Figure 11 exhibits very good noise, output impedance, and long term drift performance. It can be used in applications which have ± 15 volt supplies available. The reference has noise less than 10µV peak-to-peak from dc to 1MHz. The filtering network R2, R3, and CN filters noise components greater than 10Hz from the output of the REF10 reference. The OP-27 is a very low noise op-amp with excellent input offset drift over time and temperature.

The temperature coefficient of this reference is primarily due to the matching of the voltage divider R2 and R3, assuming that an appropriate low leakage capacitor is chosen for CN. Matched, low temperature drift resistors should be used when absolute accuracy is required. Temperature drift of the reference chip plus input offset drift



* Can be operated from +12 or +15 volts if R1 is changed to 2K.

Reference Type	Bandgap
Untrimmed Accuracy	30mV
Max Impedance	50 Ω @600Hz
Total Output Drift	30ppm/ °C
PSRR (50Hz to 500Hz)	85dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	91dB

Figure 12. -TL431 Shunt Reference

of the op-amp is about 9ppm/°C. Other 10 volt references can be used in place of the REF10.

The reference voltage can be changed by adjusting R2 and R3 according to the following equation. Vref = Vout∗(R3/(R2+R3)).

This circuit has no protection against accidentally applying ± 15V to the VREF pin. This could occur if the OP27 fails.

For applications where good dynamic performance is required, but only moderate dc accuracy, the TL431 shunt reference is an inexpensive solution. Figure 12 shows an example circuit, along with the excellent dynamic performance numbers.

Miscellaneous Applications Information

Noise from the voltage reference element may reduce system performance. Bandgap references tend to generate much more noise than zener diodes. To obtain the best noise performance from the reference element, it should be band-limited. Note the broadband noise for the LT1019-5 circuit (Figure 4, 250µV) versus the noise of a similar bandgap reference with additional circuitry to band-limit the noise as in the Great Reference (Figure 11, 10µV).

Thermal temperature gradients due to power dissipation on the voltage reference die can create output voltage shifts. Keeping the entire chip on an isothermal plane is helpful. Reference load conditions should be kept very close to those specified, or degraded temperature performance will result. Some references specify a thermal regulation in ppm/mW. This can be used to calculate voltage drift for a specific power dissipation due to loading.

Overall die temperature change can cause thermally induced output voltage variations which can exceed electrical effects. Shifts in power dissipation on the board level are the major contributor to this error. In critical applications, using a heat-sink is recommended to keep the reference temperature deviations small.

Thermocouple effects between package leads can also cause excessive output voltage drift and noise. Differences between materials in IC leads and PC-board traces can cause thermoelectric effects. Ambient air turbulence around the leads causes mismatches in the temperature between the package leads. The resulting thermoelectric voltage contributes to noise. Using dual in-line packages (DIPs) is recommended over using TO-5 type packages. The copper or Alloy 42 lead frames on DIPs are much less sensitive to thermocouple effects than the Kovar leads of the TO-5 packages. Using an enclosure such as a polysulfone shield which blocks the air flow over the reference package will also reduce the problem by reducing air movement around the package leads.

In reference circuits which have external gain setting resistors, tracking of the temperature coefficients of these resistors is vital. Wirewound resistors made of Evenohm or Mangamin have the lowest temperature coefficients. Ceramic film resistors such as Vishay are also good. Matching in resistor temperature coefficients as good as 0.4 ppm/°C can be achieved. Arranging these resistors in close proximity to one another also helps matching. SIP or DIP resistors by Beckman and Vishay exhibit the best matching since all resistors are processed on the same substrate.

Reference	Type	Untrimmed Accuracy	Maximum Impedance	Output Drift	PSRR (50Hz to 100Hz)
LT1019-5	Bandgap	2.5mV	6.5 Ω @ 3.2kHz	5ppm / °C	90dB
LT1019-4.5	Bandgap	3.0mV	3.1Ω @ 6.1kHz	5ppm / °C	90dB
LT1019-2.5	Bandgap	1.25mV	4.0Ω @ 5.8kHz	5ppm / °C	90dB
LT1021-5	Zener	2.5mV	3.8Ω @ 5.0kHz	3ppm / °C	86dB
VRE104	Zener	500µV	2.5Ω @ 20kHz	0.5ppm / °C	100dB
Low Supply	Bandgap	1.5mV	4.4Ω @ 1kHz	8ppm / °C	60dB
Low Headroom	Bandgap	50mV	6.9Ω @ 2kHz	25ppm / °C	80dB
Great	Bandgap	25mV	0.5Ω @ 3kHz	9ppm / °C	95dB
TL431 Shunt	Bandgap	30mV	50Ω @ 600Hz	30ppm / °C	85dB

Reference	Long Term Stability*	Output Noise (dc to 1MHz)	S/(N+D) (100Hz)	S/(N+D) (1kHz)
LT1019-5	-	250µV p-p	89dB	89dB
LT1019-4.5	-	150µV p-p	91dB	90dB
LT1019-2.5	-	100µV p-p	87dB	86dB
LT1021-5	15ppm / 1000hr	60µV p-p	90dB	90dB
VRE104	6ppm / 1000hr	80µV p-p	90dB	90dB
Low Supply	-	400µV p-p	88dB	88dB
Low Headroom	-	30µV p-p	90dB	90dB
Great	50ppm / 1000hr	10µV p-p	92dB	92dB
TL431 Shunt	-	100µV p-p	92dB	91dB

*Taken from reference data sheets. All other parameters were measured.

Performance Comparison Table